

What is claimed is:

- 1 1. A data processing apparatus, comprising:  
2 a first pipeline having a data cache and an instruction cache;  
3 a second pipeline coupled to the data cache and the instruction cache; and  
4 a data value prediction module coupled to the second pipeline.
- 1 2. The data processing apparatus of claim 1, further comprising:  
2 a first instruction fetch module coupled to the first pipeline; and  
3 a second instruction fetch module coupled to the second pipeline.
- 1 3. The data processing apparatus of claim 2, further comprising:  
2 a branch predictor coupled to the first and second instruction fetch modules.
- 1 4. The data processing apparatus of claim 1, further comprising:  
2 a first register file coupled to the first pipeline; and  
3 a second register file coupled to the second pipeline.
- 1 5. The data processing apparatus of claim 1, wherein the first pipeline is  
2 included in a first processor, and wherein the second pipeline is included in a second  
3 processor.
- 1 6. The data processing apparatus of claim 1, wherein the first and second  
2 pipelines are included in a single processor.
- 1 7. The data processing apparatus of claim 6, wherein the data cache, the  
2 instruction cache, and the data value prediction module are included in the single  
3 processor.
- 1 8. The data processing apparatus of claim 1, further comprising:  
2 a value prediction table coupled to the value prediction module.

1 9. The data processing apparatus of claim 1, further comprising:  
2 a main memory coupled to the data cache, wherein the first pipeline may  
3 operate to store a data value to the main memory, and wherein the second pipeline  
4 may not operate to store the data value to the main memory.

1 10. The data processing apparatus of claim 1, further comprising:  
2 a storage buffer coupled to the second pipeline.

1 11. The data processing apparatus of claim 1, further comprising:  
2 a synchronization mechanism coupled to the second pipeline.

1 12. The data processing apparatus of claim 11, wherein the synchronization  
2 mechanism includes a misprediction counter.

1 13. A computer, comprising:  
2 a first processor including a first pipeline having a data cache coupled to a  
3 memory, and an instruction cache;  
4 a second pipeline coupled to the data cache and the instruction cache; and  
5 a data value prediction module coupled to the second pipeline.

1 14. The computer of claim 13, further comprising:  
2 a second processor including the second pipeline.

1 15. The computer of claim 13, further comprising:  
2 a bus coupled to the data cache and the memory, wherein the first processor  
3 includes the second pipeline.

1 16. The computer of claim 13, further comprising:  
2 a value prediction table coupled to the value prediction module.

1 17. The computer of claim 13, further comprising:

2 a synchronization mechanism coupled to the second pipeline.

1 18. The computer of claim 17, wherein the synchronization mechanism includes  
2 a run-ahead counter.

1 19. The data processing apparatus of claim 13, further comprising:  
2 a storage buffer coupled to the second pipeline.

1 20. An article comprising a machine-accessible medium having associated data,  
2 wherein the data, when accessed, results in a machine performing:  
3 executing a plurality of instructions including a LOAD instruction using a  
4 first pipeline sharing an instruction cache and a data cache with a second pipeline;  
5 calculating a predicted load value for execution of the LOAD instruction if a  
6 cache miss in the data cache results when the second pipeline executes the LOAD  
7 instruction before the first pipeline; and  
8 continuing execution of the plurality of instructions using the second  
9 pipeline.

1 21. The article of claim 20, wherein the machine-accessible medium further  
2 includes data, which when accessed by the machine, results in the machine  
3 performing:  
4 counting a number of mispredictions occurring when the predicted load  
5 value is incorrect; and  
6 restarting execution of the plurality of instructions by the second pipeline at  
7 a program counter value maintained by the first pipeline if the number of  
8 mispredictions is greater than or equal to a preselected threshold value.

1 22. The article of claim 20, wherein the machine-accessible medium further  
2 includes data, which when accessed by the machine, results in the machine  
3 performing:

4 counting a number of instructions included in the plurality of instructions  
5 which the second pipeline has executed ahead of the first pipeline; and  
6 restarting execution of the plurality of instructions by the second pipeline at a  
7 program counter value maintained by the first pipeline if the number of instructions  
8 is greater than or equal to a preselected threshold value.

1 23. The article of claim 20, wherein the machine-accessible medium further  
2 includes data, which when accessed by the machine, results in the machine  
3 performing:  
4 beginning execution of the plurality of instructions by the first and second  
5 pipelines at a same program counter value.

1 24. A method of processing data, comprising:  
2 executing a plurality of instructions including a LOAD instruction using a  
3 first pipeline sharing an instruction cache and a data cache with a second pipeline;  
4 calculating a predicted load value for execution of the LOAD instruction if a  
5 cache miss in the data cache results when the second pipeline executes the LOAD  
6 instruction before the first pipeline; and  
7 continuing execution of the plurality of instructions using the second  
8 pipeline.

1 25. The method of claim 24, further comprising:  
2 counting a number of mispredictions occurring when the predicted load  
3 value is incorrect; and  
4 restarting execution of the plurality of instructions by the second pipeline at  
5 a program counter value maintained by the first pipeline if the number of  
6 mispredictions is greater than or equal to a preselected threshold value.

1 26. The method of claim 24, further comprising:  
2 counting a number of instructions included in the plurality of instructions  
3 which the second pipeline has executed ahead of the first pipeline; and

4 restarting execution of the plurality of instructions by the second pipeline at  
5 a program counter value maintained by the first pipeline if the number of  
6 instructions is greater than or equal to a preselected threshold value.

1 27. The method of claim 24, further comprising:  
2 beginning execution of the plurality of instructions by the first and second  
3 pipelines at a same program counter value.